

HSF Property:ROHS

ACER
BAP41/BAP51/BAP52/BXP41/SJM52
UMA+Discrete(SW Gfx)
MAIN BOARD

2009.06.30

Tuesday, June 30, 2009		A02
DATE	CHANGE NO.	REV

<http://laptop-motherboard-schematic.blogspot.com/>

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE			
DESIGN					BAP41/BAP51 (Montevina SFF)			
CHECK					SIZE			
RESPONSIBLE					CODE			
					DOC NUMBER			
					D-CS-1310A2282001-ALG			
					SHEET			
					1 of 48			

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal

18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRIII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)
24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

31. LCD/CRT

32. KBC ITE8502E-L

33. IO CN

34. IO CN

35. IO CN

36. Audio Codec

37. EASY PORT CN/ LEVEL SHIFTER

38. M92-S2(1/5)

39. M92-S2(2/5)

40. M92-S2(3/5)

41. M92-S2(4/5)

42. M92-S2(5/5)

43. DDR3 VRAM

44. HyBrid Switch

45. dGPU Power

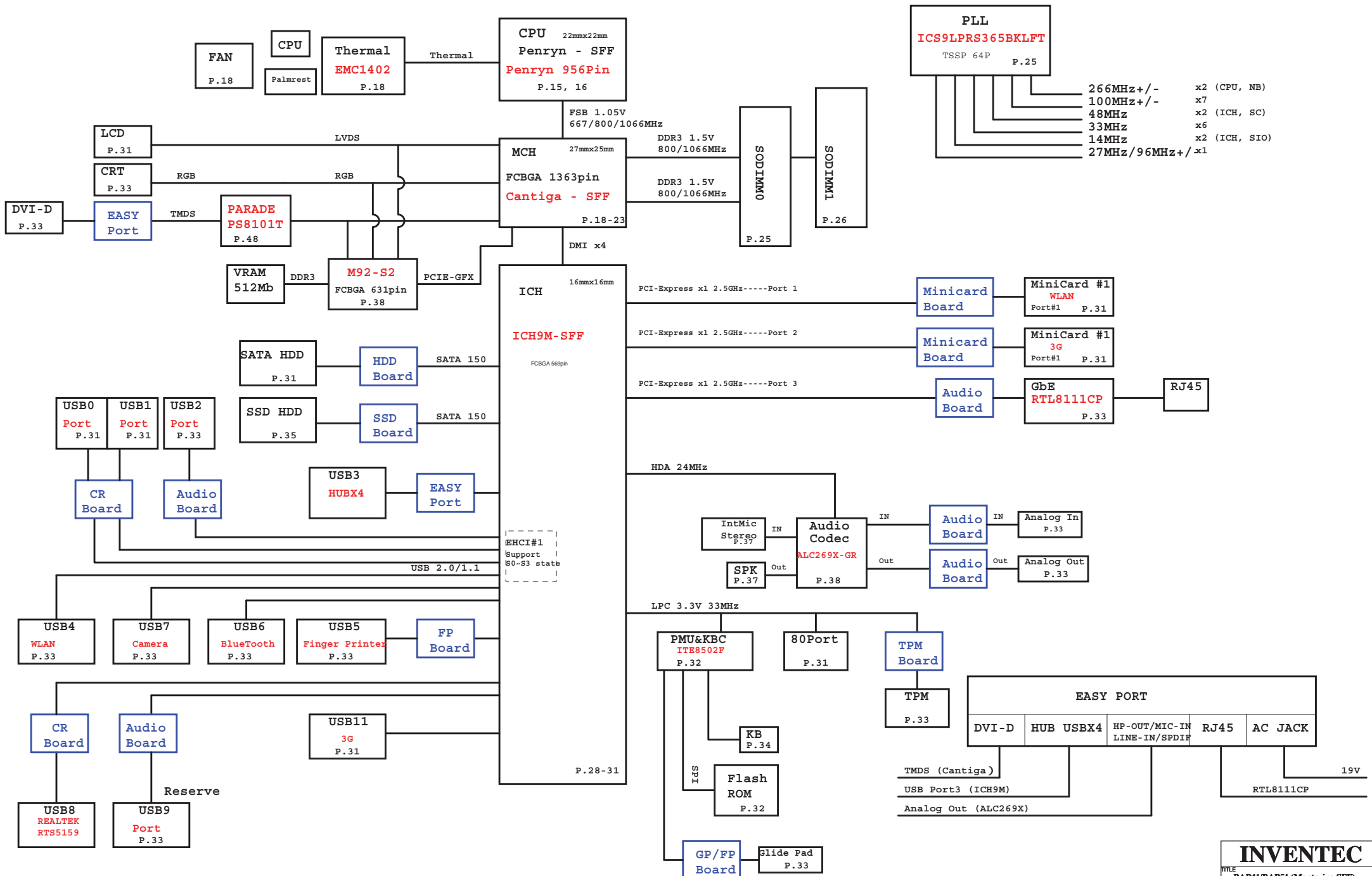
46. dGPU Power

47. dGPU Power

48. HDD Board

49. TPM Board

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R

VCC CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R

+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions









C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII:DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC62 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF)			
ANNOTATIONS			
SIZE Custom	CODE A02	DOC NUMBER D-CS-1310A2292001-ALG	REV A02
SHEET 4 of 49			

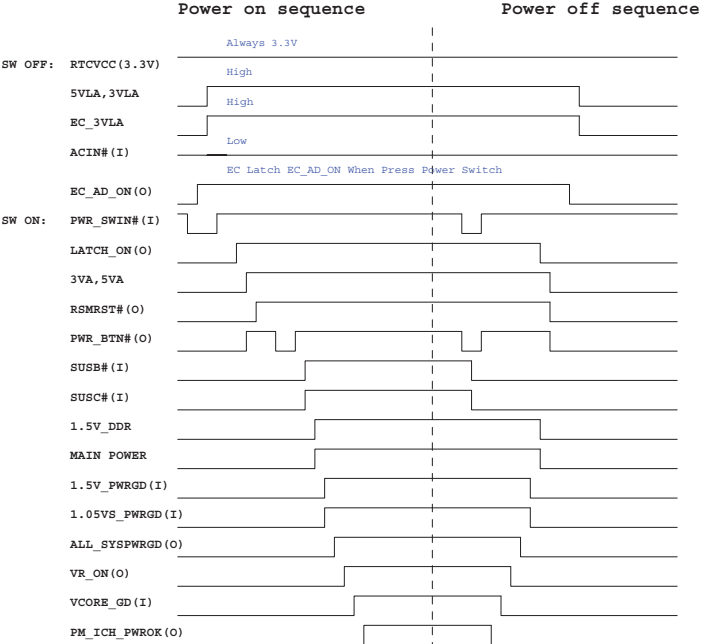
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<http://laptop-motherboard-schematic.blogspot.com/>

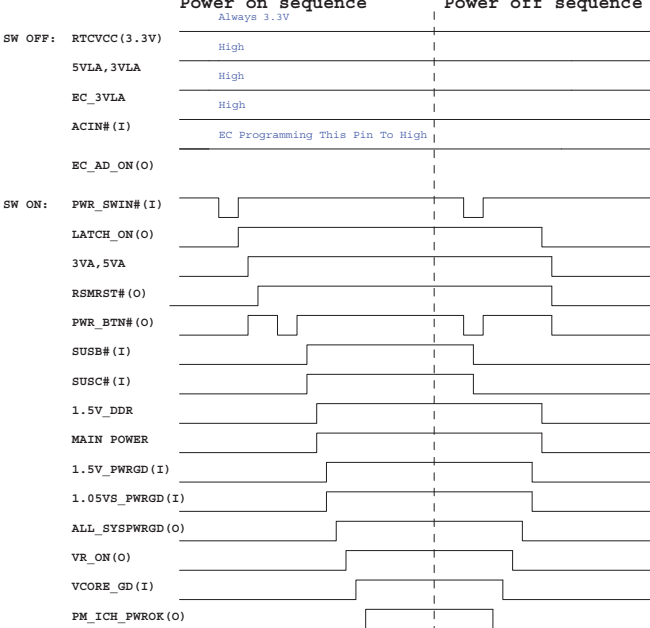
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TITLE BAP41/BAP51 (Montevina SFT)			
Schematic Modify			
SIZE Custom	CODE A02	DOC NUMBER D-CS-1310A2292001-ALG	REV A02
SHEET		5	of 49

SYSTEM POWER ON/OFF SEQUENCE

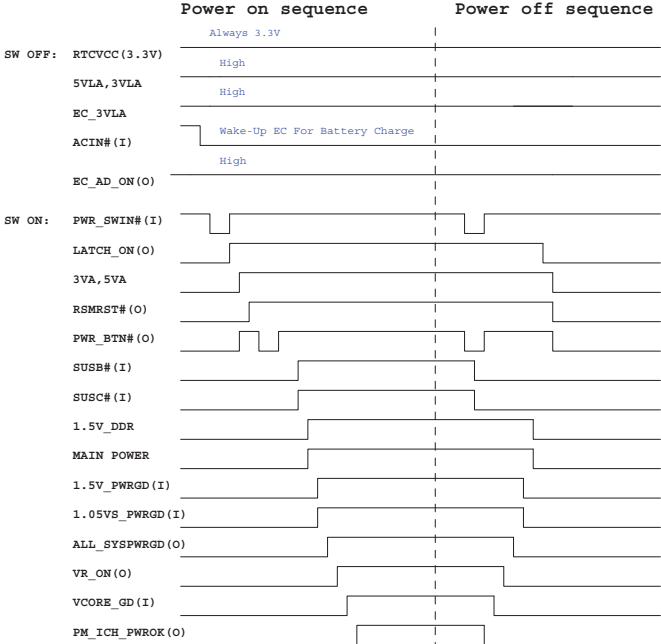
Power on/off sequence AC insert (without Battery Pack)



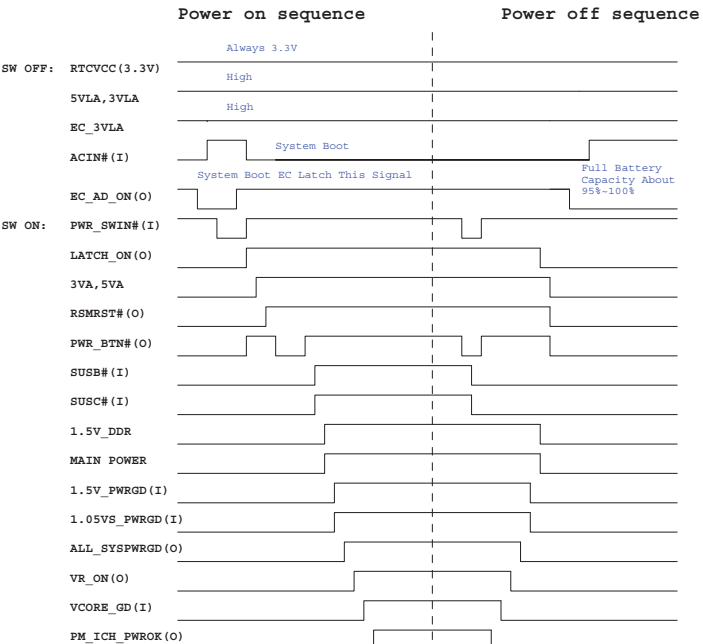
Power on/off sequence Battery insert (without AC adapter)



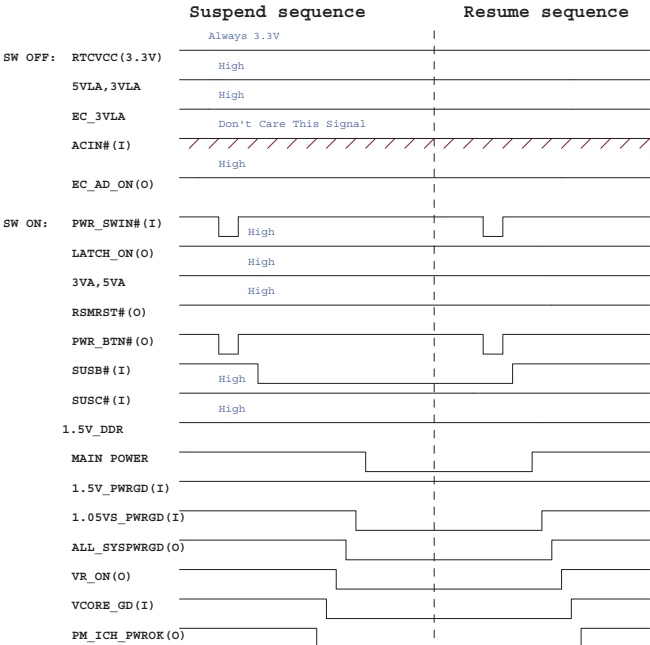
Power on/off sequence AC insert (with charge over 95%)



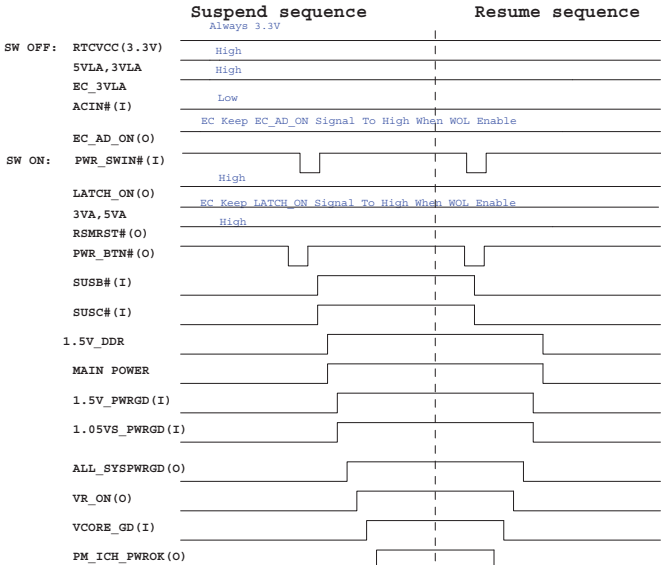
Power on/off sequence AC insert (without charge over 95%)



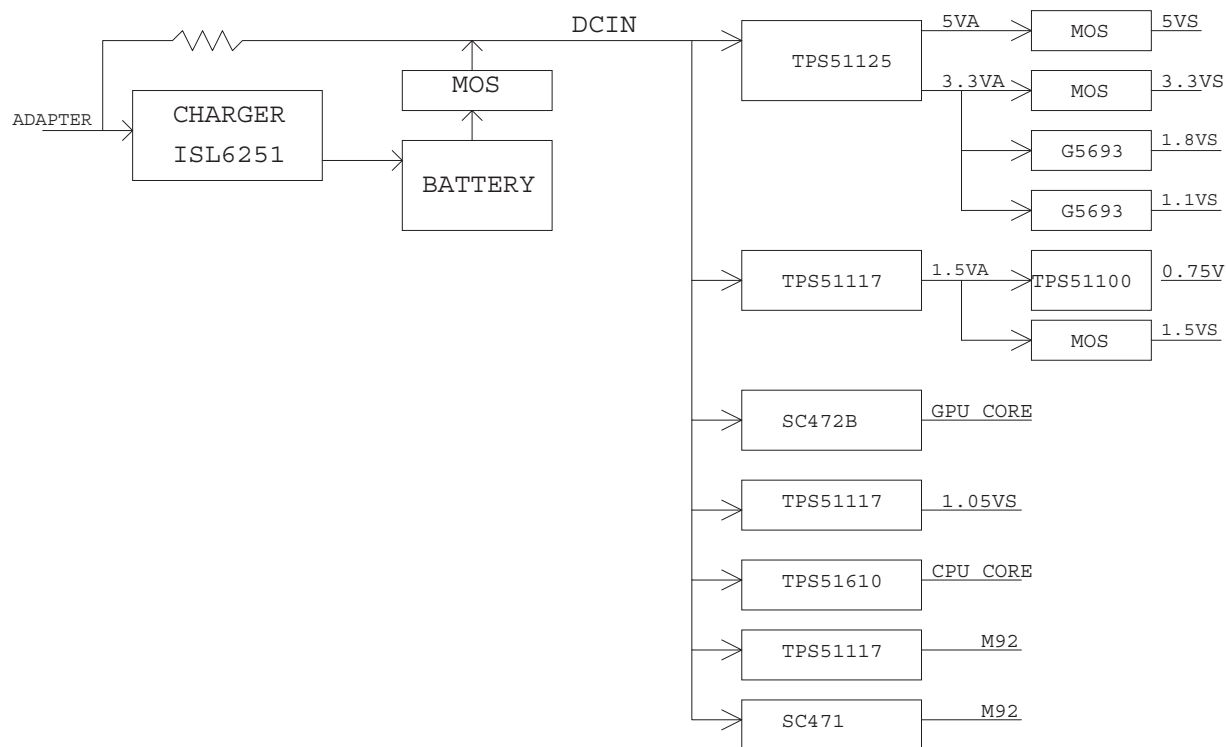
Suspend And Resume Sequence (S3)



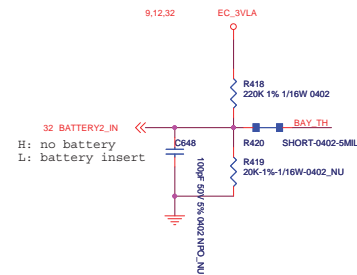
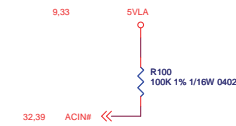
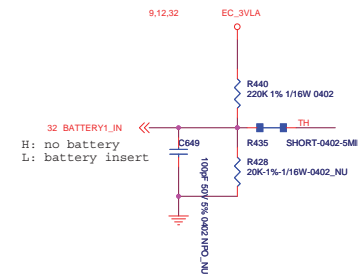
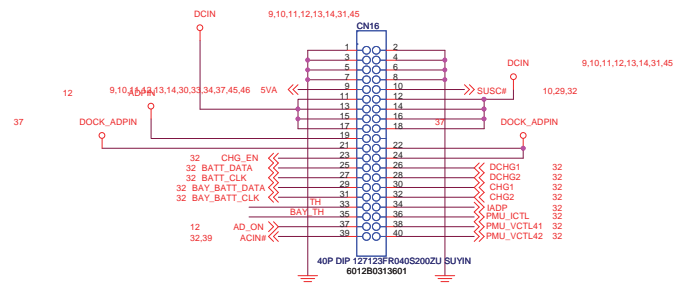
Power on/off sequence after windows shoutdown (WOL enable)



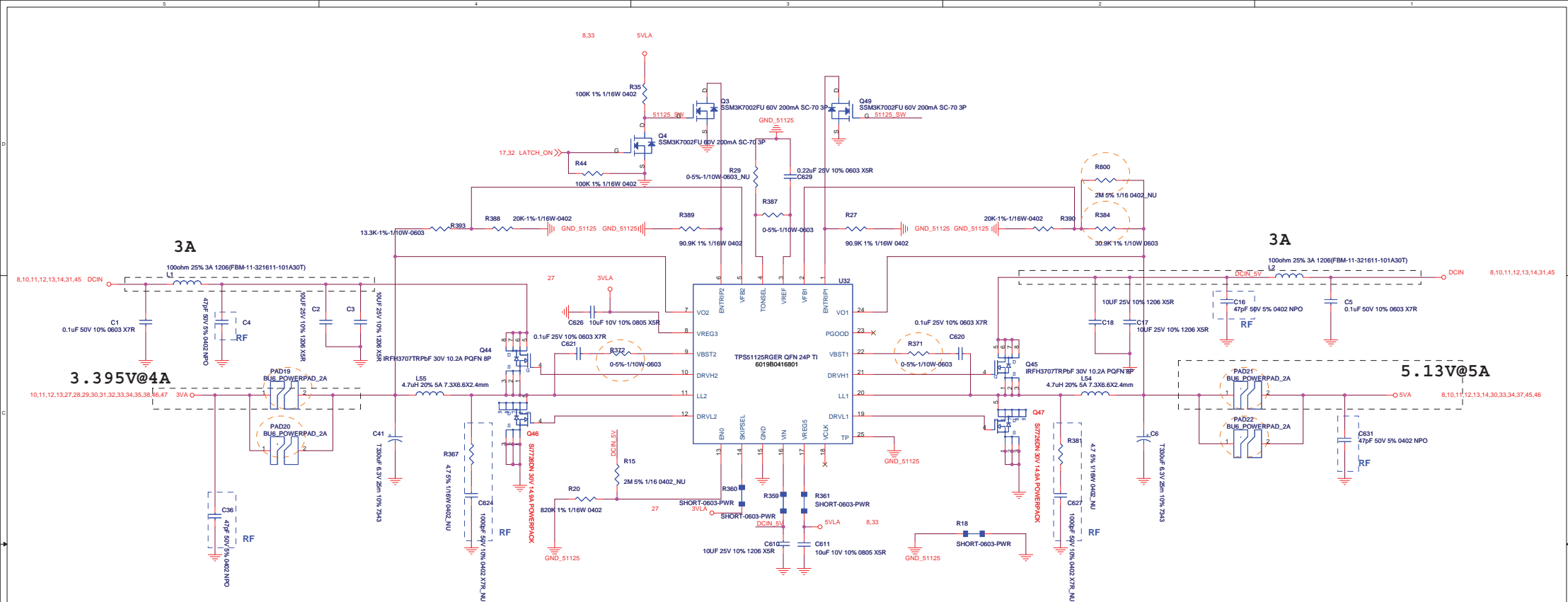
Power Block Diagram :



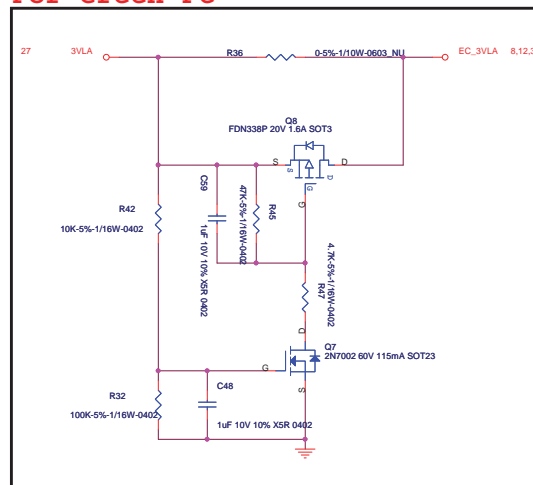
Charger CN TO USIM/B



INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF)			
Adapter In / Charge			
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02
SHEET		8	49

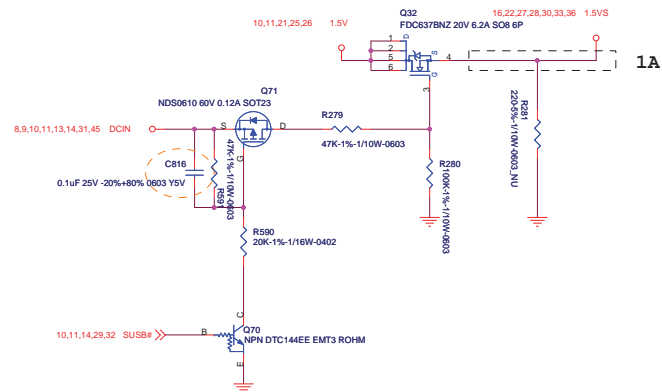


For Green PC

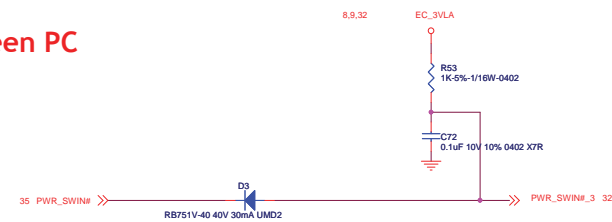


INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF)			
SVLA/SVA/3VLA/3VA			
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02
SHEET		8 of 49	

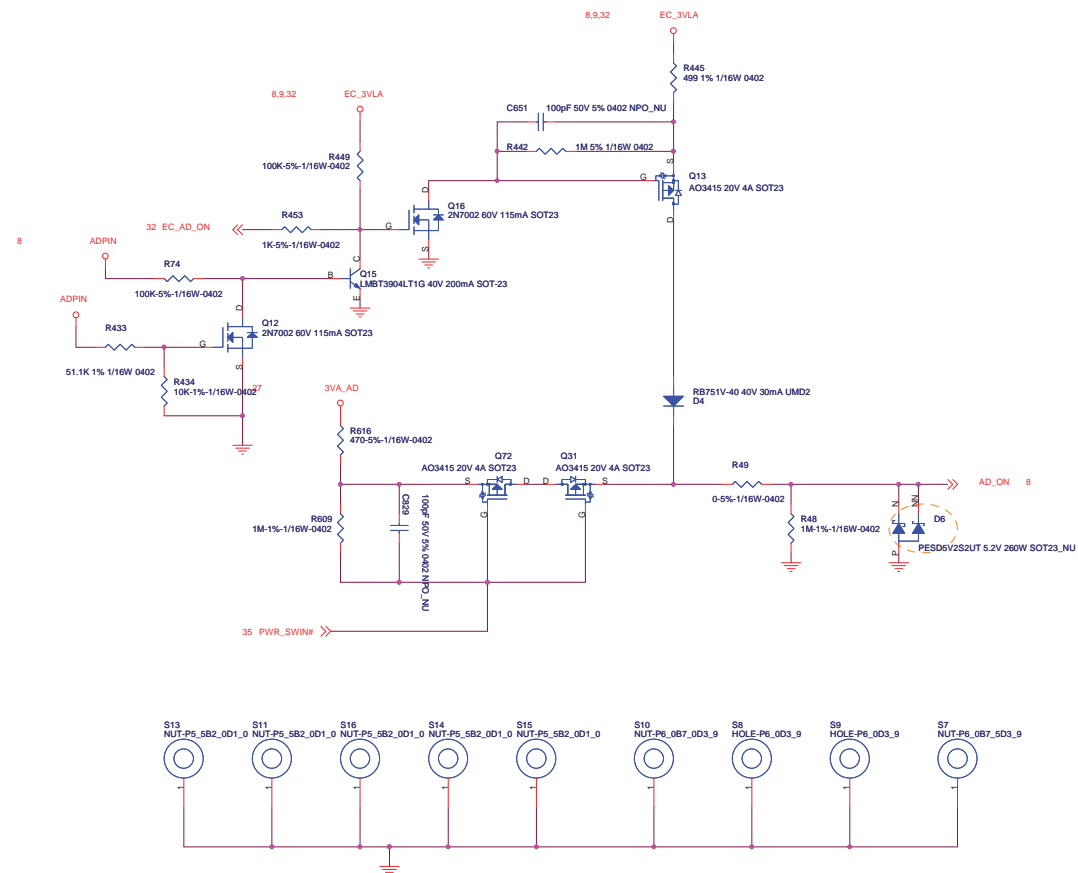
1.5VS



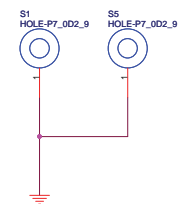
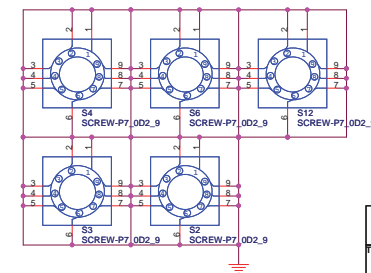
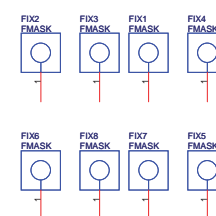
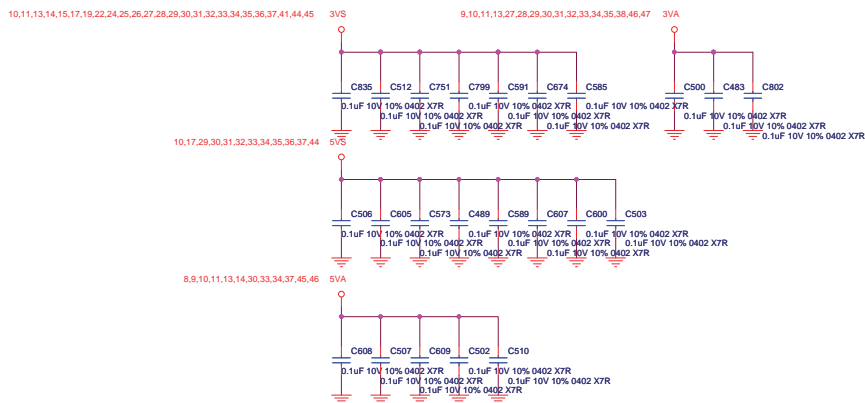
For Green PC



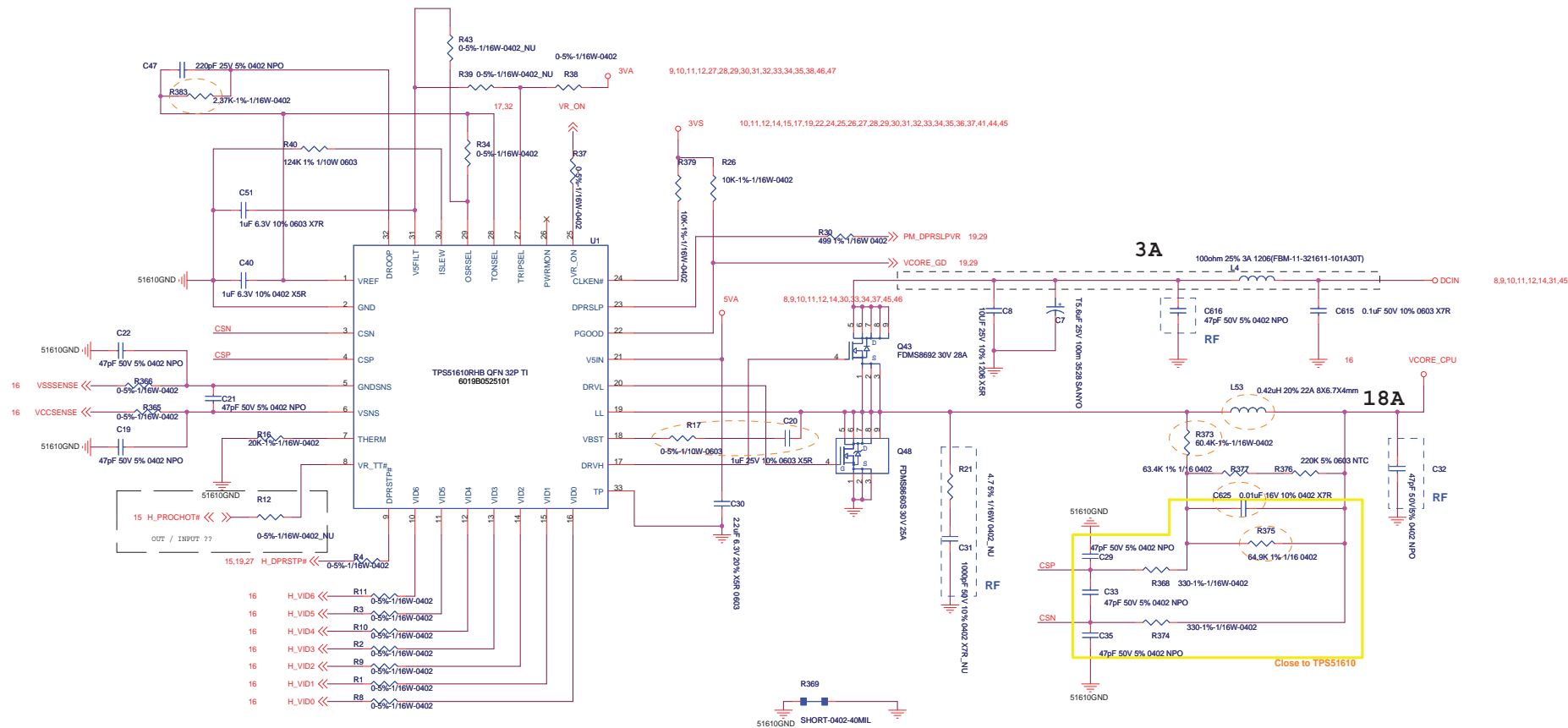
None Green PC ---- NU

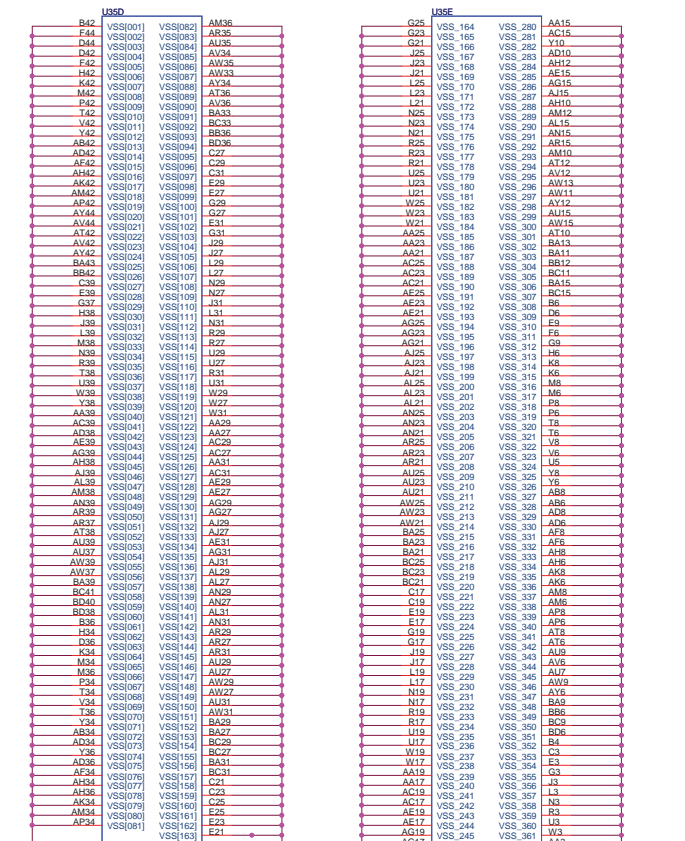


EMI Cap



INVENTEC			
TITLE: BAP41/BAP51 (Montevina SFF)			
Power on latch			
SHEET	CODE	DOC NUMBER	REV
Custom	A02	D-C8-1310A2292001-ALG	A02
DATE		Thursday, July 02, 2009	
SHEET		12 of 49	





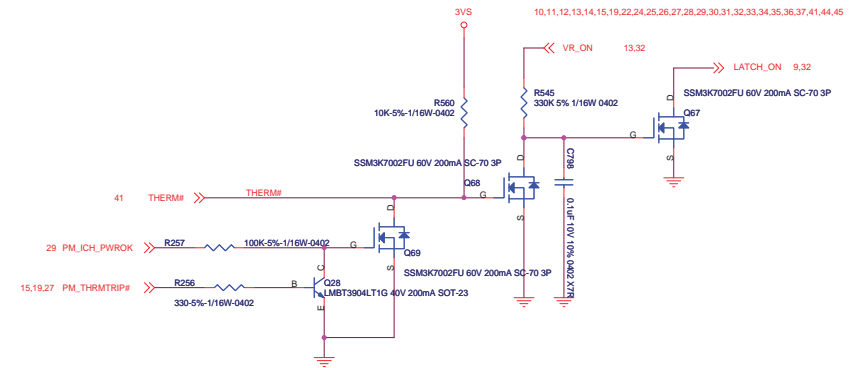
The diagram shows the pin configuration for XDP P/U & P/D. It includes a dashed box containing the following pins and their connections:

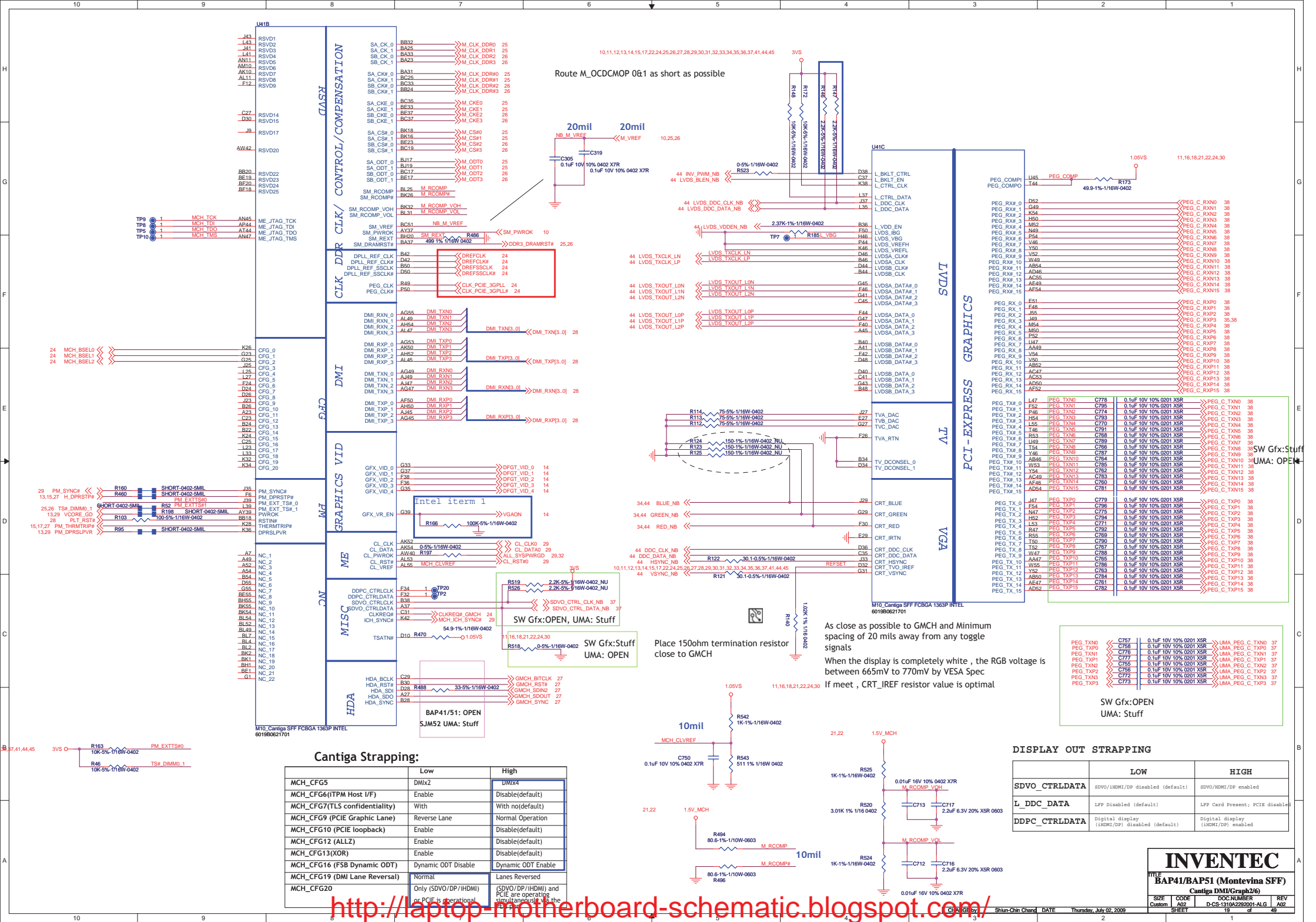
- XDP_DBRESET#** (R76) connected to 1K5Ω-1/16W-0402 and 3VS.
- XDP_TDO** (R385) connected to 54.9-1% 1/16W-0402.
- XDP_TMS** (R24) connected to 54.9-1% 1/16W-0402 and CPU 16.
- XDP_TDI** (R25) connected to 54.9-1% 1/16W-0402.
- XDP_TCLK** (R482) connected to 54.9-1% 1/16W-0402.
- XDP_TRST#** (R22) connected to 649-1% 1/16W-0402.
- XDP_TCK** (R378) connected to 54.9-1% 1/16W-0402.

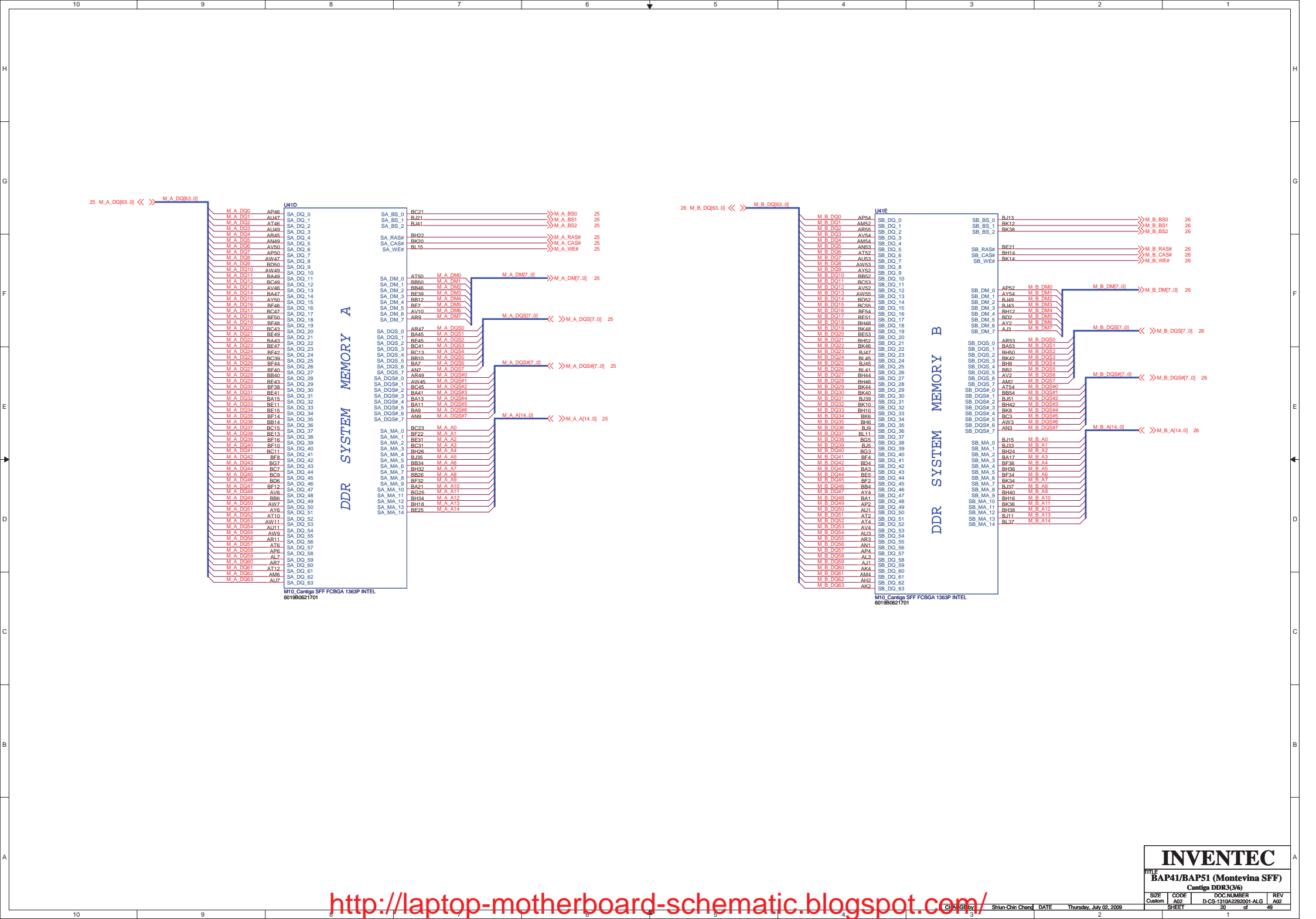
A ground symbol is shown at the bottom right of the dashed box.

H_D[63..0]		H_D[63..0]		H_D[63..0]		H_D[63..0]	
	H_D[0]	F40	J038				
	H_D[1]	G43	D11				
	H_D[2]	E45	D39				
	H_D[3]	J43	D39				
	H_D[4]	H40	D49				
	H_D[5]	H46	D39				
	H_D[6]	H46	D39				
	H_D[7]	E41	D77				
	H_D[8]	L45	D99				
	H_D[9]	K44	D99				
	H_D[10]	N41	D109				
	H_D[11]	T40	D109				
	H_D[12]	M40	D109				
	H_D[13]	G41	D109				
	H_D[14]	M44	D109				
	H_D[15]	L43	D109				
18	H_D[STBN0]		D[STBN]0				
18	H_D[STBN1]		D[STBN]1				
18	H_D[STBN2]		D[STBN]2				
18	H_D[STBN3]		D[STBN]3				
18	H_D[STBN4]		D[STBN]4				
18	H_D[STBN5]		D[STBN]5				
18	H_D[STBN6]		D[STBN]6				
18	H_D[STBN7]		D[STBN]7				
18	H_D[STBN8]		D[STBN]8				
18	H_D[STBN9]		D[STBN]9				
18	H_D[STBN10]		D[STBN]10				
18	H_D[STBN11]		D[STBN]11				
18	H_D[STBN12]		D[STBN]12				
18	H_D[STBN13]		D[STBN]13				
18	H_D[STBN14]		D[STBN]14				
18	H_D[STBN15]		D[STBN]15				
18	H_D[STBN16]		D[STBN]16				
18	H_D[STBN17]		D[STBN]17				
18	H_D[STBN18]		D[STBN]18				
18	H_D[STBN19]		D[STBN]19				
18	H_D[STBN20]		D[STBN]20				
18	H_D[STBN21]		D[STBN]21				
18	H_D[STBN22]		D[STBN]22				
18	H_D[STBN23]		D[STBN]23				
18	H_D[STBN24]		D[STBN]24				
18	H_D[STBN25]		D[STBN]25				
18	H_D[STBN26]		D[STBN]26				
18	H_D[STBN27]		D[STBN]27				
18	H_D[STBN28]		D[STBN]28				
18	H_D[STBN29]		D[STBN]29				
18	H_D[STBN30]		D[STBN]30				
18	H_D[STBN31]		D[STBN]31				
18	H_D[STBN32]		D[STBN]32				
18	H_D[STBN33]		D[STBN]33				
18	H_D[STBN34]		D[STBN]34				
18	H_D[STBN35]		D[STBN]35				
18	H_D[STBN36]		D[STBN]36				
18	H_D[STBN37]		D[STBN]37				
18	H_D[STBN38]		D[STBN]38				
18	H_D[STBN39]		D[STBN]39				
18	H_D[STBN40]		D[STBN]40				
18	H_D[STBN41]		D[STBN]41				
18	H_D[STBN42]		D[STBN]42				
18	H_D[STBN43]		D[STBN]43				
18	H_D[STBN44]		D[STBN]44				
18	H_D[STBN45]		D[STBN]45				
18	H_D[STBN46]		D[STBN]46				
18	H_D[STBN47]		D[STBN]47				
18	H_D[STBN48]		D[ST				

Comp0,2 connect with $Z_0=27.4\Omega$, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with $Z_0=55\Omega$, make trace length shorter than 0.5" and width is 5mils

[illegible]

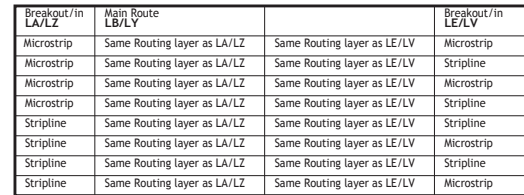







```

graph LR
    subgraph SMCH
        Tx1[Tx]
        Rx1[Rx]
    end
    subgraph ICH8m
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --> LA1[LA1]
    LA1 --> LA2[LA2]
    LA2 --> LB[LB]
    LB --> LC[LC]
    LC --> LD[LD]
    LD --> LE[LE]
    LE --> Rx2
    Rx2 --> LZ1[LZ1]
    LZ1 --> LZ2[LZ2]
    LZ2 --> LY[LY]
    LY --> LX[LX]
    LX --> LW[LW]
    LW --> LV[LV]
    LV --> Tx1
  
```

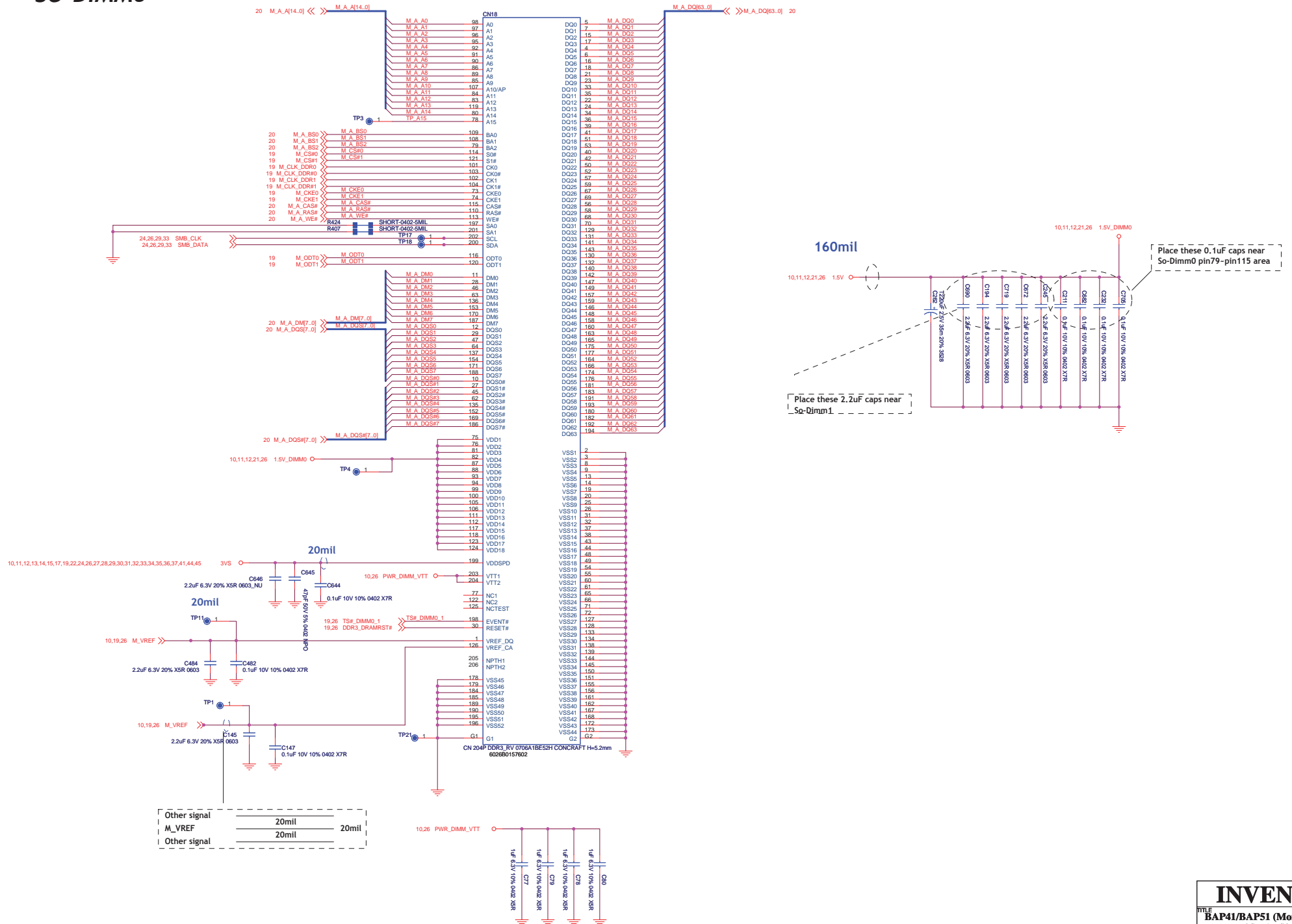


*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

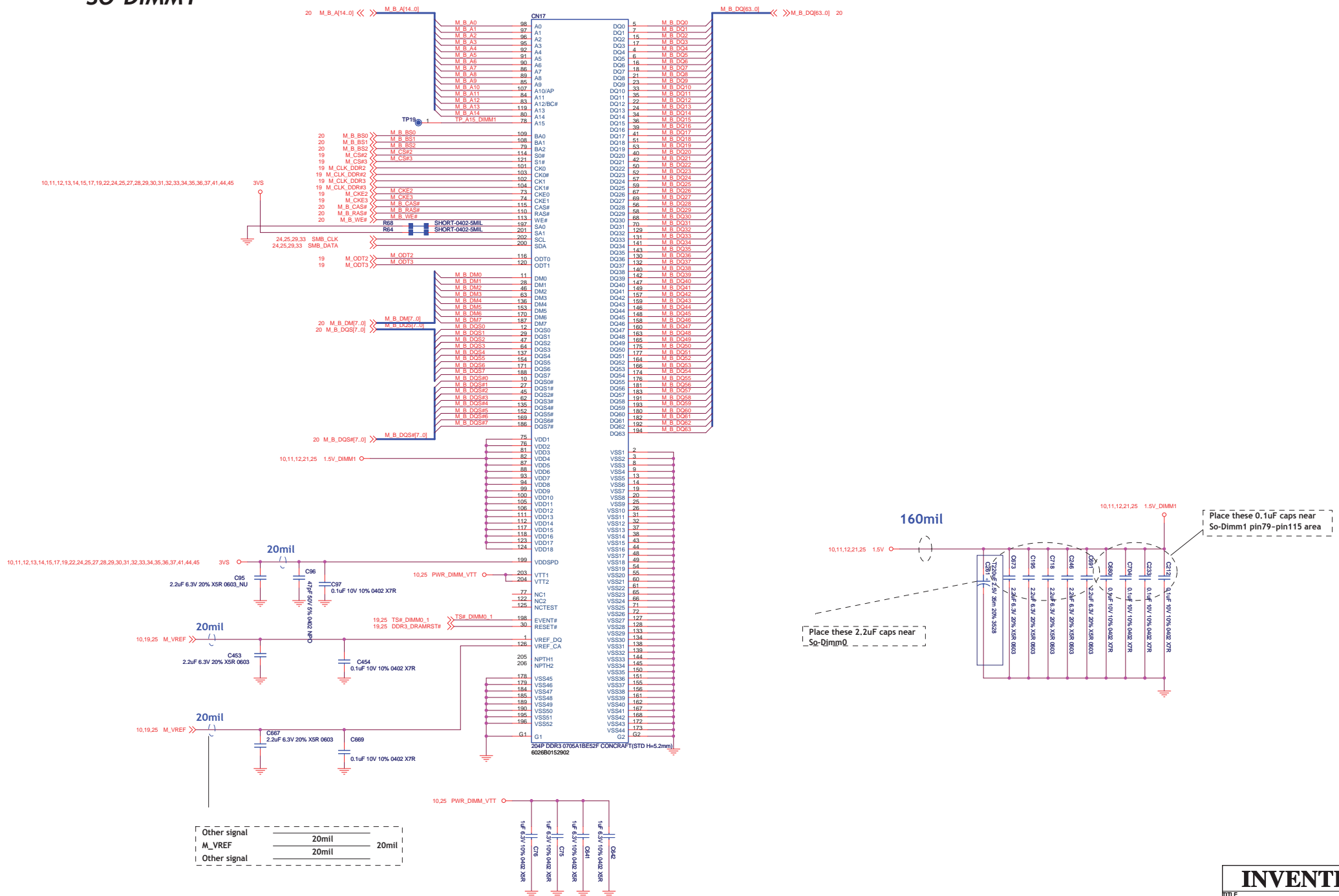


SIZE Custom	CODE A02	DOC. NUMBER D-CS-1310A2292001-ALG	REV A02
SHEET		23 of	49

SO-DIMM0



SO-DIMM 1

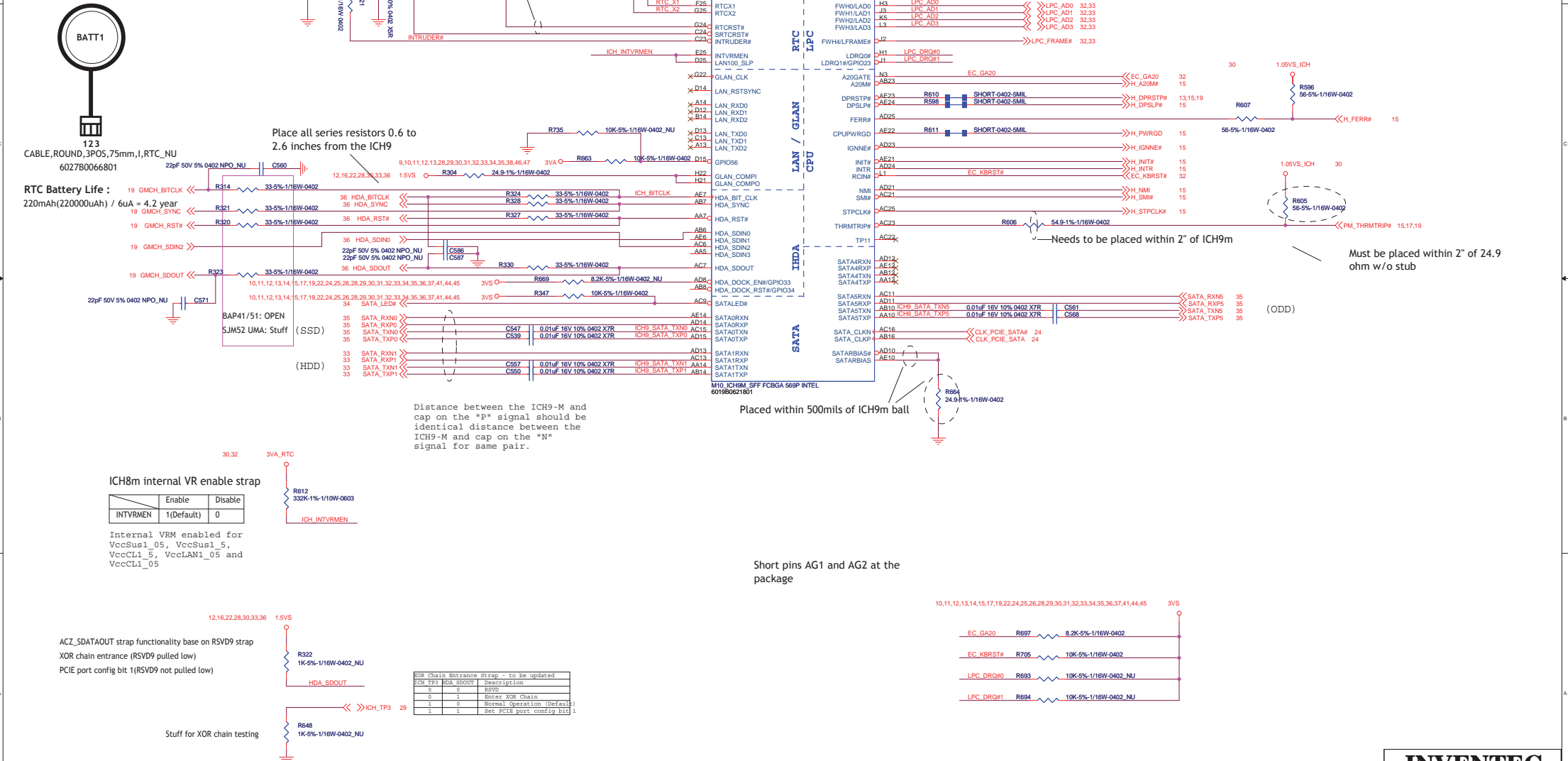


RTC Circuit

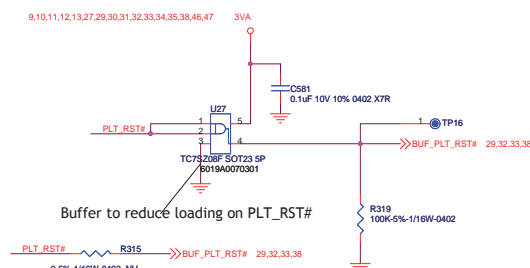
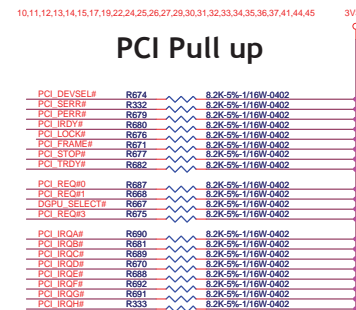
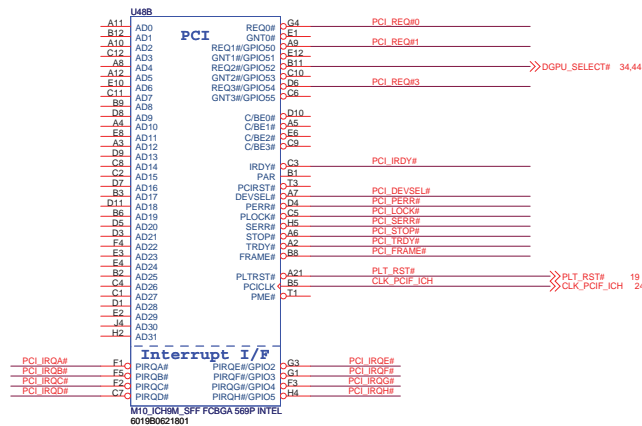
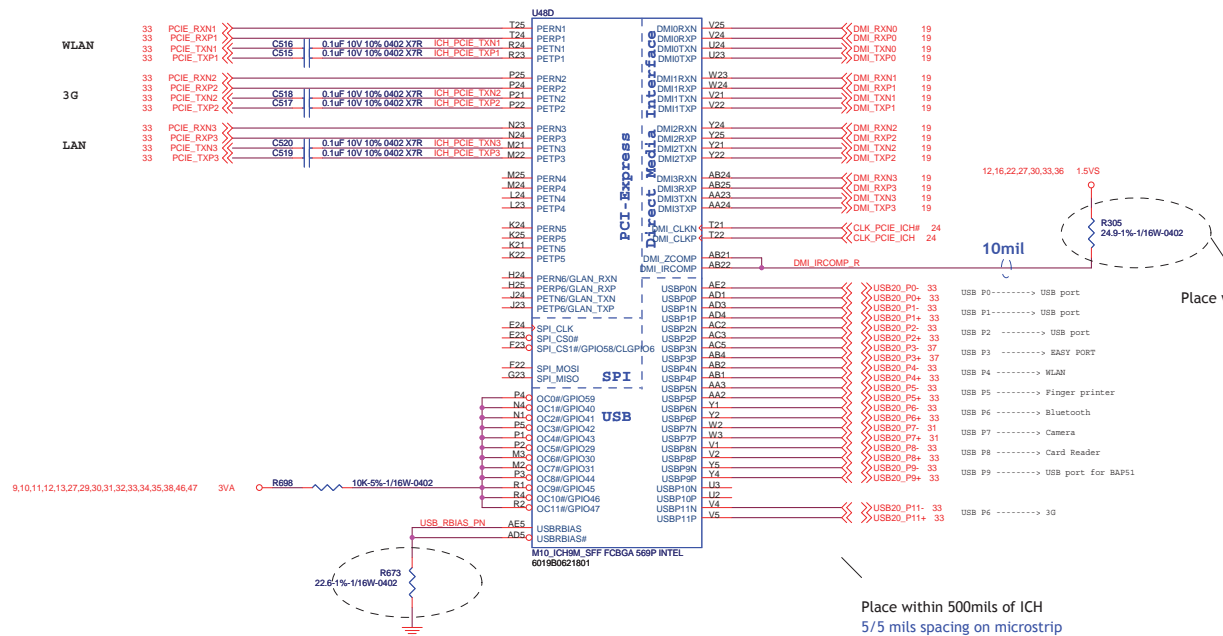
1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

For Green PC



PCIE AC coupling caps need to be within 250mils of the driver

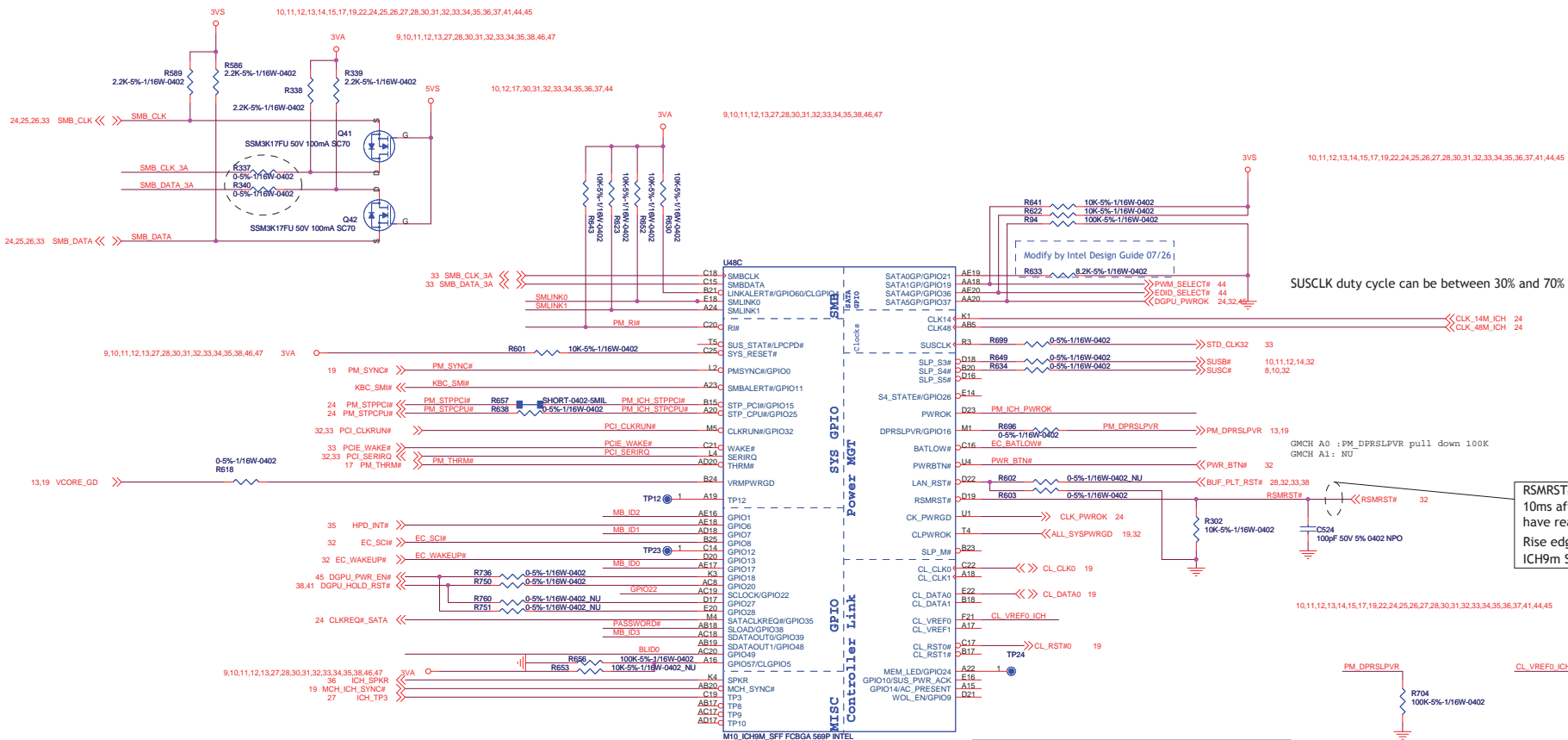


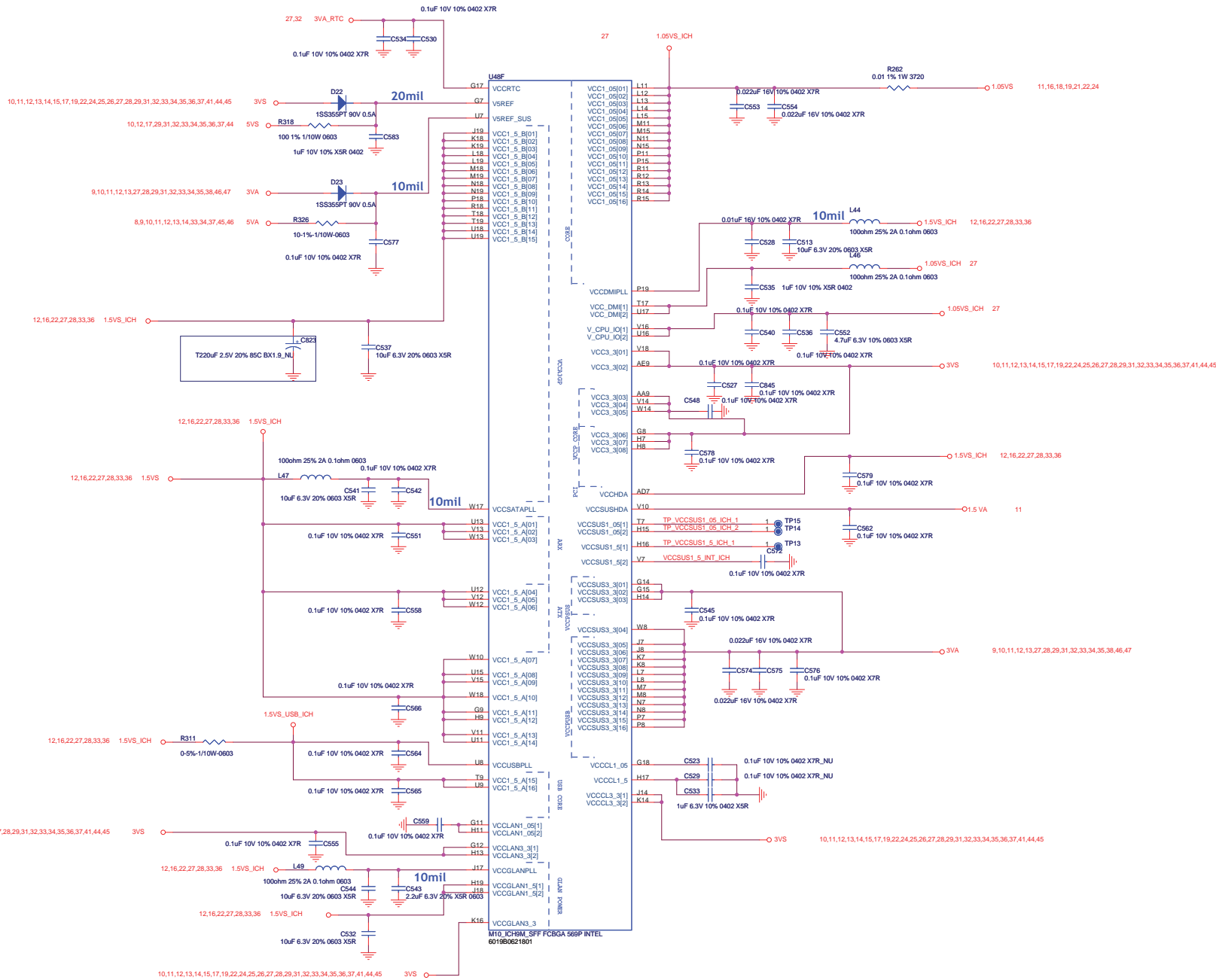
PCI_GNT#3 No stuff : by default
Stuff : For A16 swap override

PCI_GNT#0	SPL_CS1#
1	1
1	0
0	1

Check BIOS type

<http://laptop-motherboard-schematic.blogspot.com/>

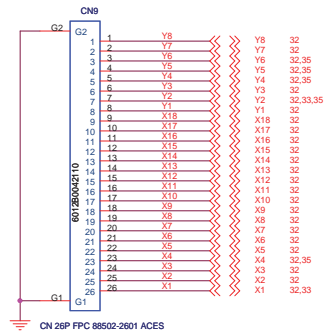




B4	VSS1001	VSS1007	U6
B10	VSS1002	VSS1008	W11
B13	VSS1003	VSS1009	W14
B14	VSS1004	VSS1010	W16
B15	VSS1005	VSS1011	U21
B18	VSS1006	VSS1012	U22
D2	VSS1007	VSS1013	U25
D24	VSS1008	VSS1014	U26
E5	VSS1009	VSS1015	V3
E7	VSS1010	VSS1016	V19
E11	VSS1011	VSS1017	W1
E12	VSS1012	VSS1018	W23
E13	VSS1013	VSS1019	W4
E14	VSS1014	VSS1020	W7
E15	VSS1015	VSS1021	W9
E17	VSS1016	VSS1022	W15
E18	VSS1017	VSS1023	W19
E21	VSS1018	VSS1024	W19
F24	VSS1019	VSS1025	W21
G2	VSS1020	VSS1026	W22
G5	VSS1021	VSS1027	W25
G10	VSS1022	VSS1028	Y3
G13	VSS1023	VSS1029	AA1
G16	VSS1024	VSS1030	AA4
G19	VSS1025	VSS1031	AA6
H10	VSS1026	VSS1032	AA8
H12	VSS1027	VSS1033	AA11
H23	VSS1028	VSS1034	AA13
J5	VSS1029	VSS1035	AA15
J6	VSS1030	VSS1036	AA17
J10	VSS1031	VSS1037	AA19
J11	VSS1032	VSS1038	AA21
J12	VSS1033	VSS1039	AA22
J13	VSS1034	VSS1040	AA24
J15	VSS1035	VSS1041	AA24
J21	VSS1036	VSS1042	AA25
J22	VSS1037	VSS1043	AA26
J25	VSS1038	VSS1044	AA27
K2	VSS1039	VSS1045	AA28
K2	VSS1040	VSS1046	AA29
K8	VSS1041	VSS1047	AA31
K10	VSS1042	VSS1048	AA32
K11	VSS1043	VSS1049	AA33
K12	VSS1044	VSS1050	AA34
K13	VSS1045	VSS1051	AA35
K15	VSS1046	VSS1052	AA36
K17	VSS1047	VSS1053	AA37
K23	VSS1048	VSS1054	AA38
L6	VSS1049	VSS1055	AA39
L8	VSS1050	VSS1056	AA40
L10	VSS1051	VSS1057	AA41
L16	VSS1052	VSS1058	AA42
L17	VSS1053	VSS1059	AA43
L21	VSS1054	VSS1060	AA44
L22	VSS1055	VSS1061	AA45
L25	VSS1056	VSS1062	AA46
M8	VSS1057	VSS1063	AA47
M10	VSS1058	VSS1064	AA48
M12	VSS1059	VSS1065	AA49
M13	VSS1060	VSS1066	AA50
M14	VSS1061	VSS1067	AA51
M16	VSS1062	VSS1068	AA52
M17	VSS1063	VSS1069	AA53
M23	VSS1064	VSS1070	AA54
N2	VSS1065	VSS1071	AA55
N6	VSS1066	VSS1072	AA56
N8	VSS1067	VSS1073	AA57
N10	VSS1068	VSS1074	AA58
N12	VSS1069	VSS1075	AA59
N13	VSS1070	VSS1076	AA60
N14	VSS1071	VSS1077	AA61
N16	VSS1072	VSS1078	AA62
N17	VSS1073	VSS1079	AA63
N21	VSS1074	VSS1080	AA64
N22	VSS1075	VSS1081	AA65
N25	VSS1076	VSS1082	AA66
P9	VSS1077	VSS1083	AA67
P10	VSS1078	VSS1084	AA68
P12	VSS1079	VSS1085	AA69
P13	VSS1080	VSS1086	AA70
P16	VSS1081	VSS1087	AA71
P17	VSS1082	VSS1088	AA72
P23	VSS1083	VSS1089	AA73
P24	VSS1084	VSS1090	AA74
R5	VSS1085	VSS1091	AA75
R6	VSS1086	VSS1092	AA76
R7	VSS1087	VSS1093	AA77
R8	VSS1088	VSS1094	AA78
R9	VSS1089	VSS1095	AA79
R10	VSS1090	VSS1096	AA80
R16	VSS1091	VSS1097	AA81
R17	VSS1092	VSS1098	AA82
R21	VSS1093	VSS1099	AA83
R22	VSS1094	VSS1100	AA84
R25	VSS1095	VSS1101	AA85
R26	VSS1096	VSS1102	AA86
R27	VSS1097	VSS1103	AA87
T6	VSS1098	VSS1104	AA88
T10	VSS1099	VSS1105	AA89
T11	VSS1100	VSS1106	AA90
T12	VSS1101	VSS1107	AA91
T13	VSS1102	VSS1108	AA92
T14	VSS1103	VSS1109	AA93
T16	VSS1104	VSS1110	AA94
T18	VSS1105	VSS1111	AA95
T23	VSS1106	VSS1112	AA96

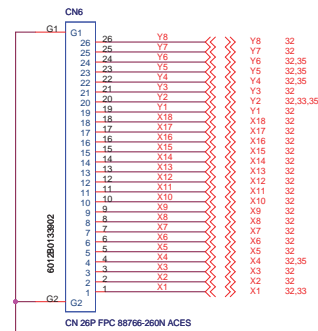


To K/B(For BAP41)



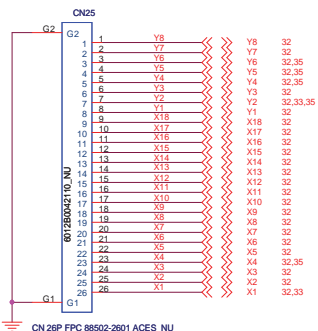
(Pin1 已反通)

To K/B (For BAP51/BAP52/SJM52)



(Pin1 已反通)

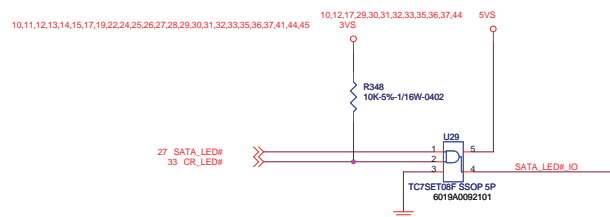
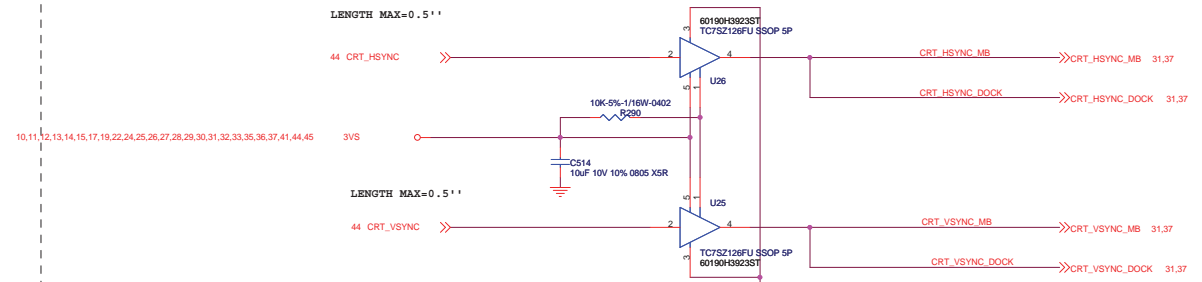
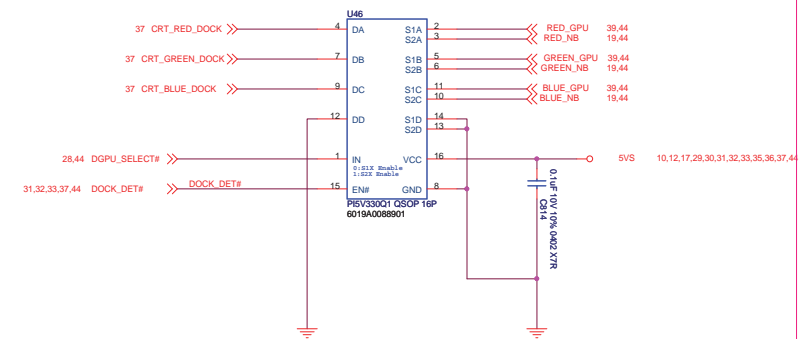
To K/B(For BXP41)



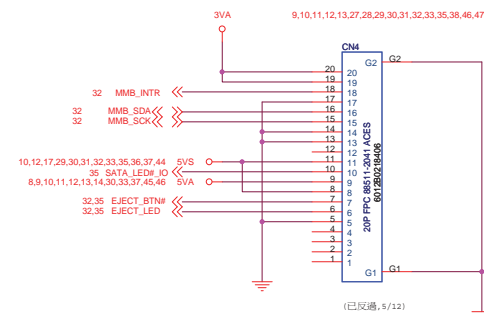
(Pin1 已反通)

BAP41/51/52/BXP41: Stuff U46,C814

SJM52 : OPEN U46,C814

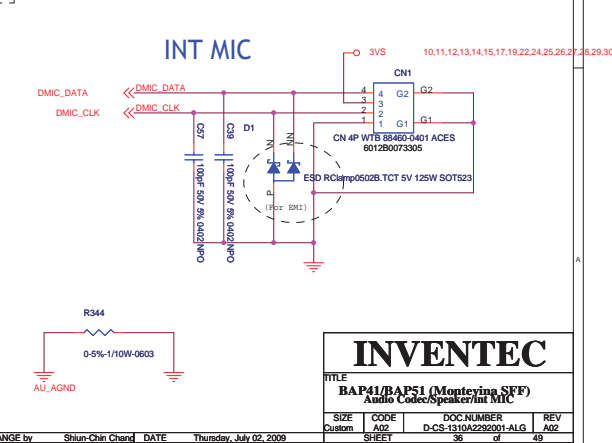
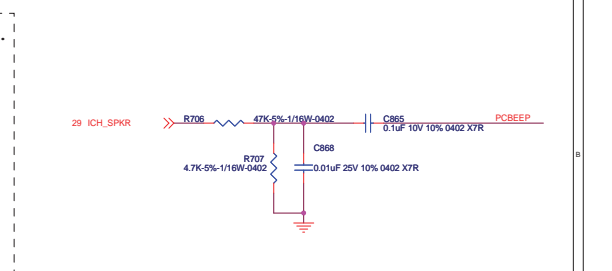
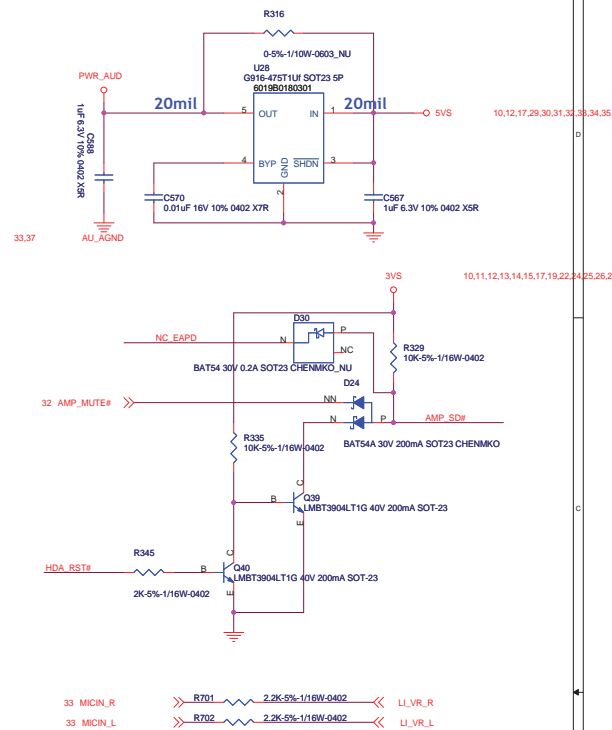


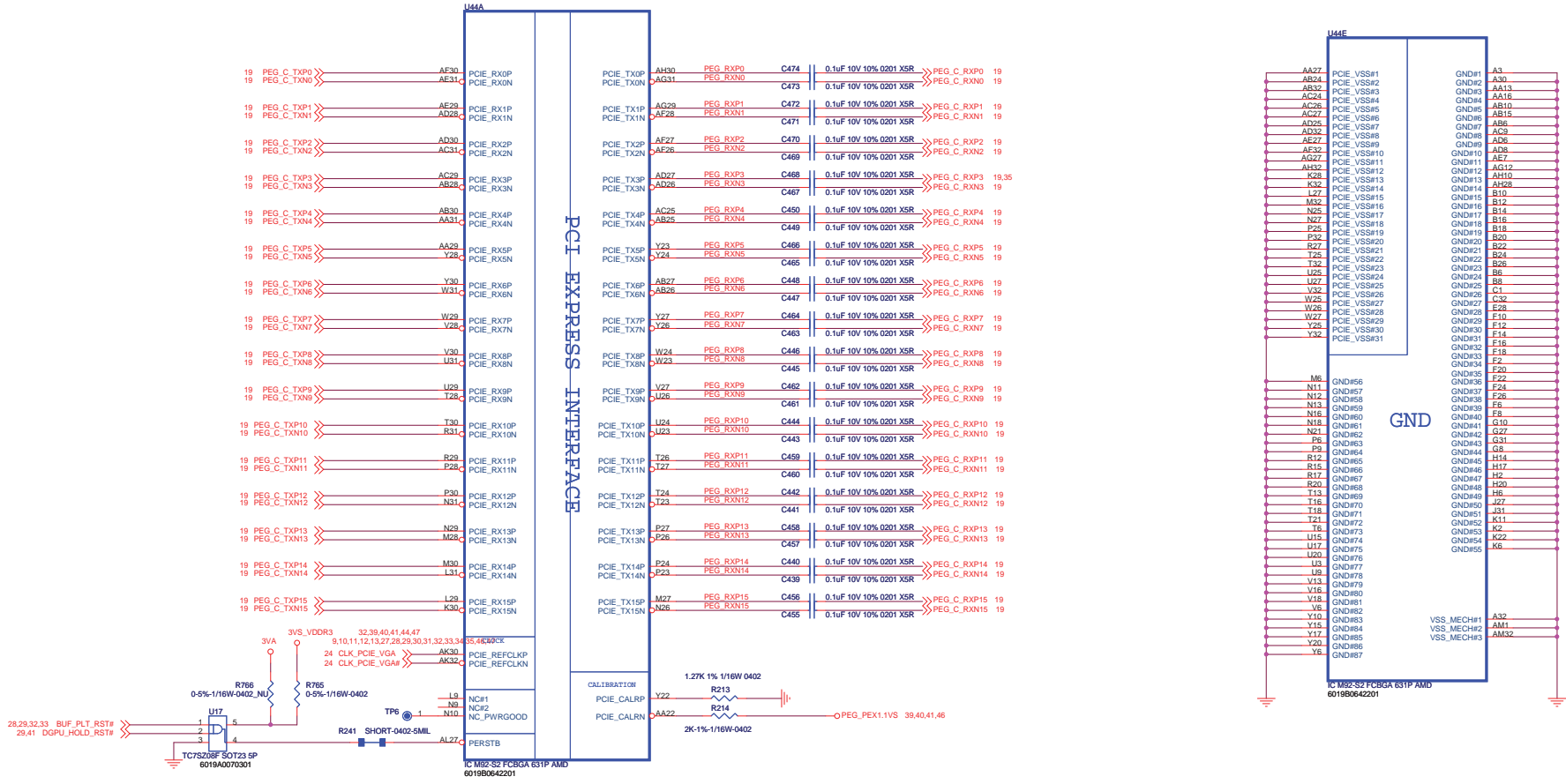
SW Sensor BOARD(For SJM52)



BAP41/51/52/BXP41: OPEN
SJM52: Stuff

INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF) BDP			
SIZE Custom	CODE A02	DOC NUMBER D-CS-1310A226001-ALG	REV A02
CHANGE by Shun-Chin Chang	DATE Thursday, July 02, 2009		





Page 38:
SW Gfx: Stuff
UMA: OPEN

INVENTEC

TITLE
BAP41/BAP51 (Montevina SFT)
M92

SIZE
Custom

CODE
A02

DOC NUMBER
D-CS-1310A2292001-ALG

REV
A02

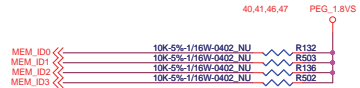
DATE
Thursday, July 02, 2009

1

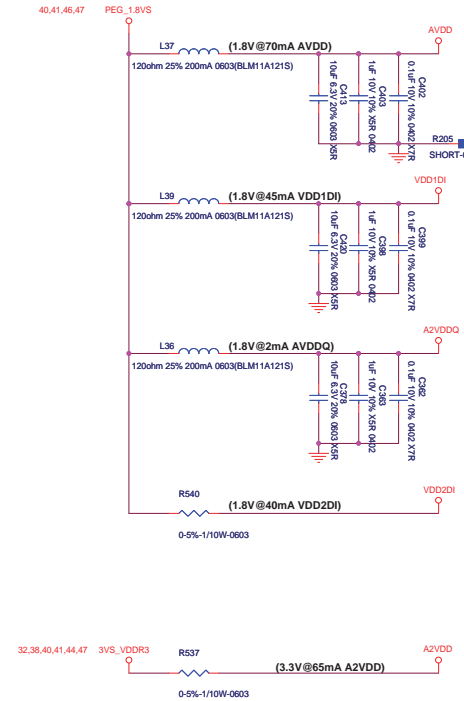
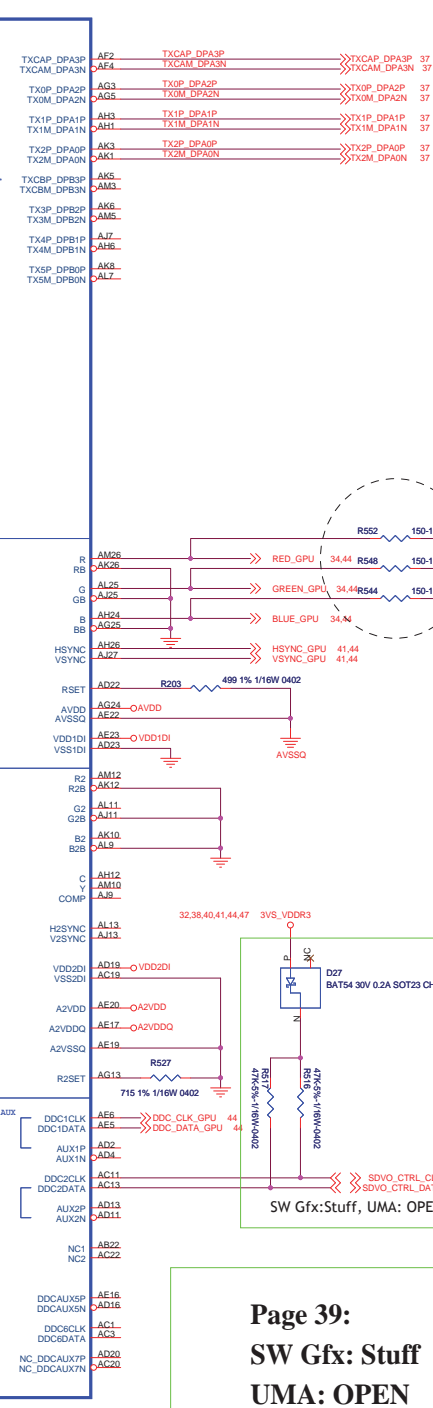
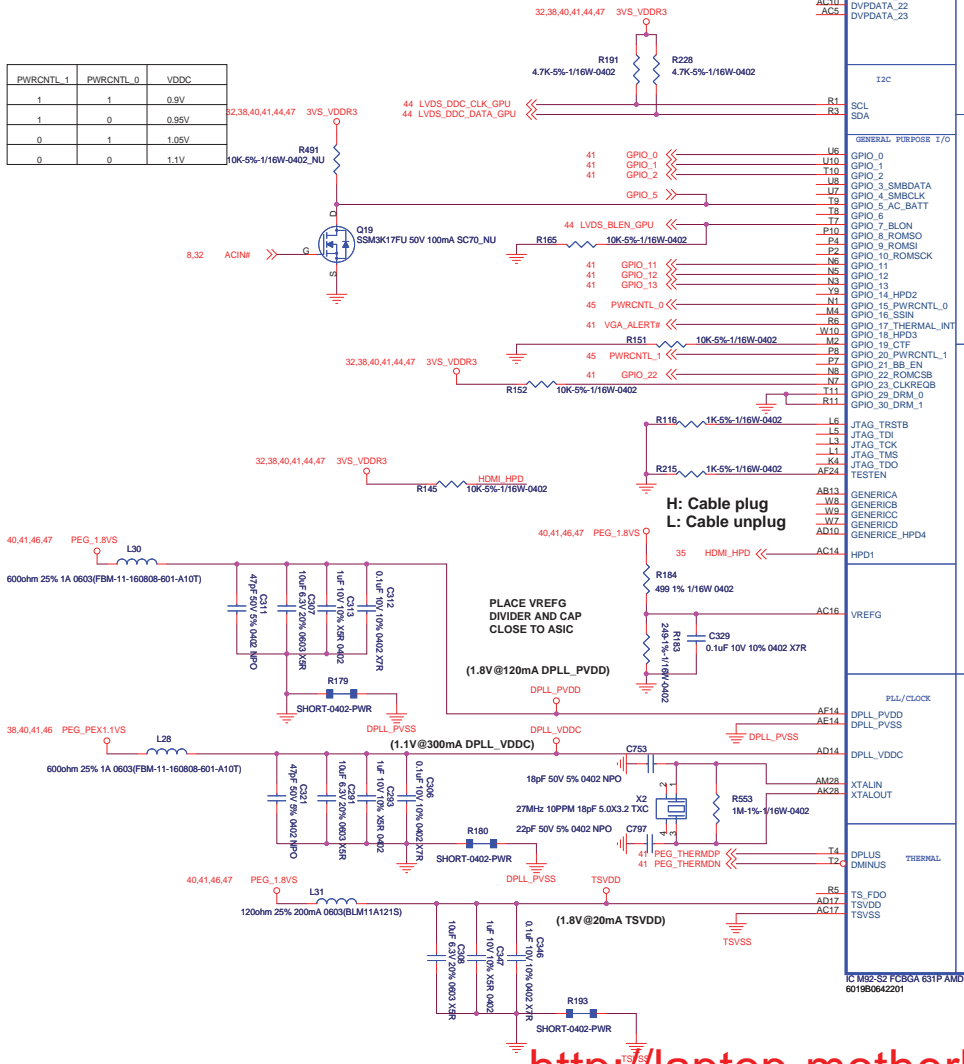
38

49

MEM ID3	MEM ID2	MEM ID1	MEM ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16



PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V



Page 39:
SW Gfx: Stuff
UMA: OPEN

U44C

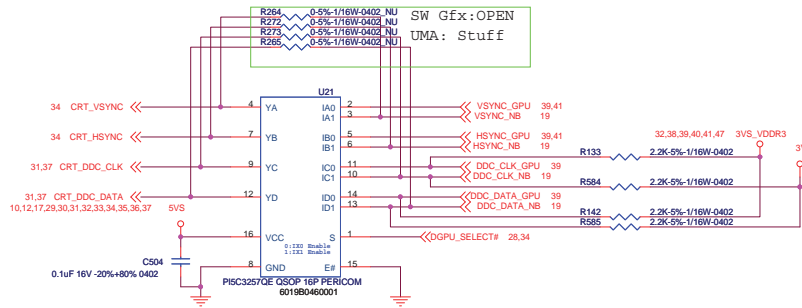


PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

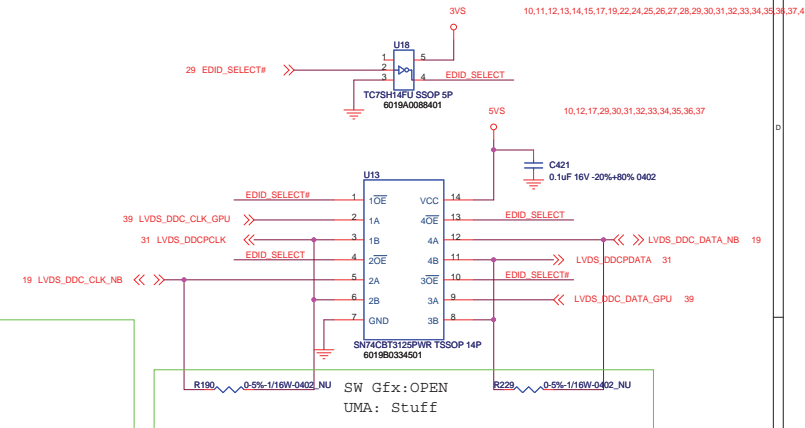


Shun-Chin Chang	DATE	Thursday
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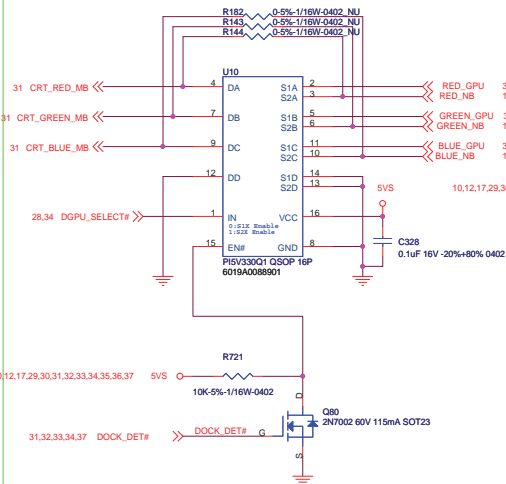
CRT HSYNC/VSNC/DDC SW



LCD DDC SW



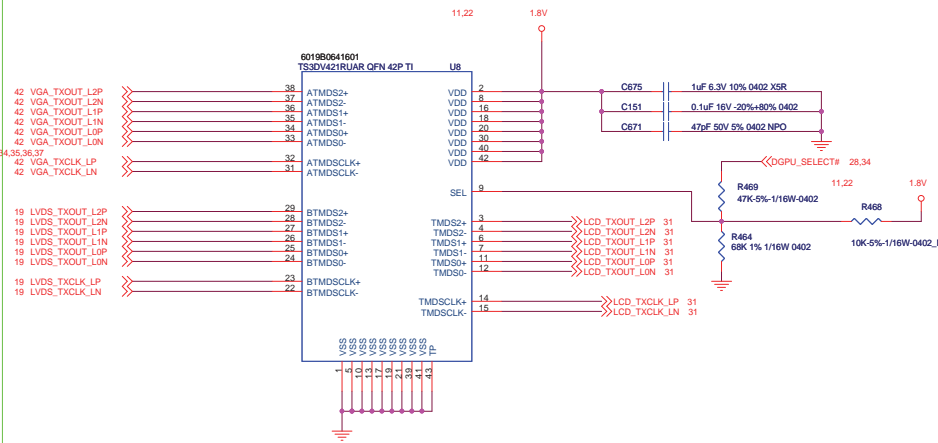
CRT R/G/B SW



Stuff CRT/RGB SW for both SW Gfx and UMA

SW Gfx : Stuff U10,C328,R721,Q80
UMA : Stuff U10,C328,R721,Q80

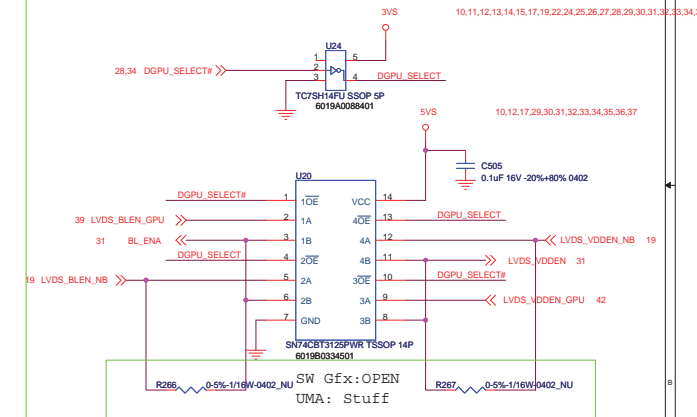
LVDS SW



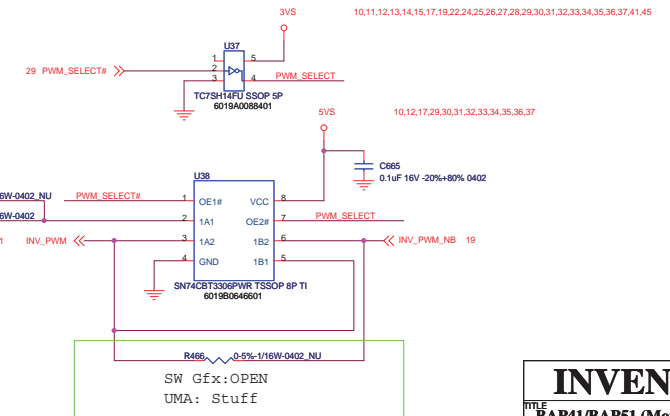
Thermal Pad limitation : Stuff LVDS SW for both SW Gfx and UMA

SW Gfx : Stuff U8,C675,C151,C671,R469,R464, OPEN R468
UMA : Stuff U8,C675,C151,C671,R468, OPEN R469,R464

LVDS BKL and Vcc Enable SW

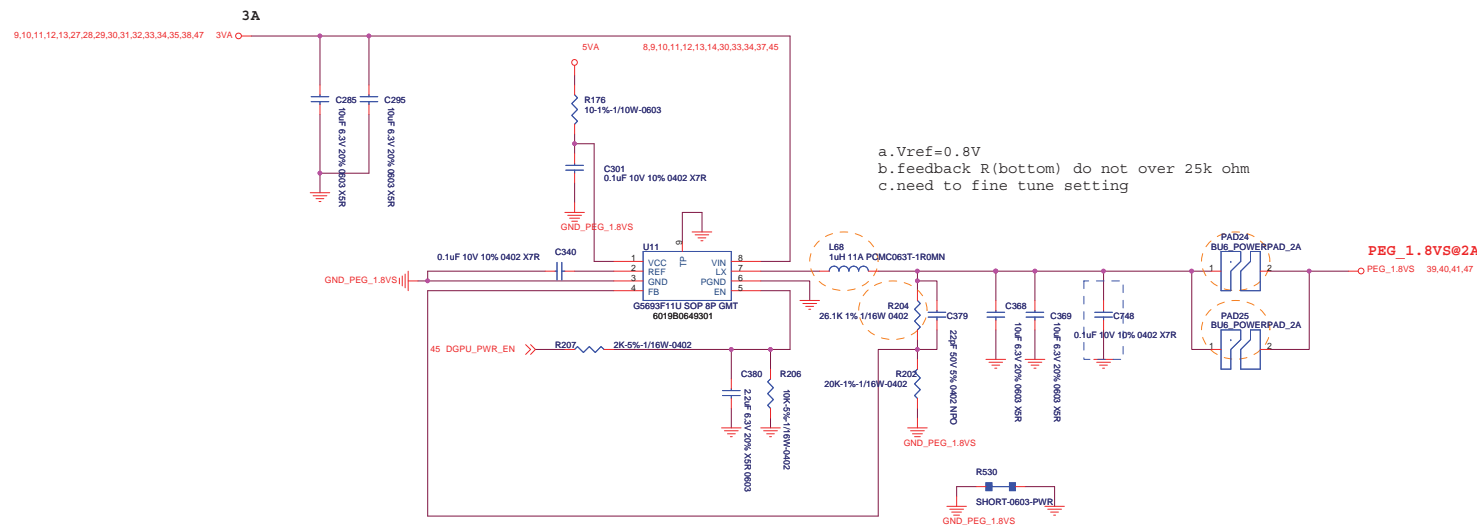


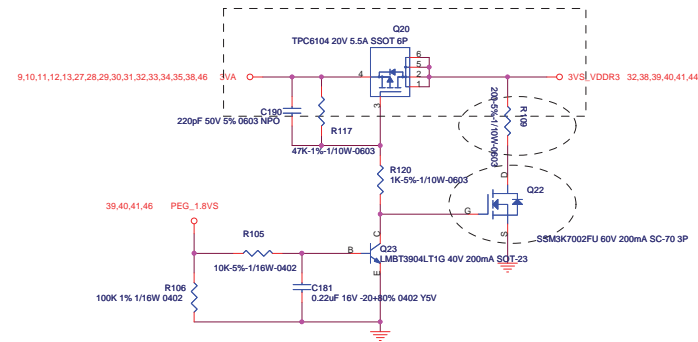
LCD PWM SW



Page 44:
SW Gfx: Stuff
UMA: OPEN

Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
EDID_SELECT#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

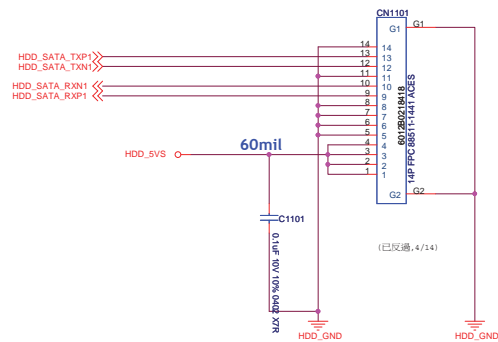




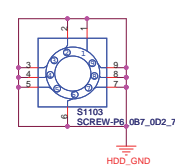
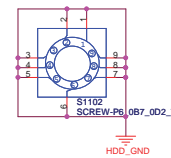
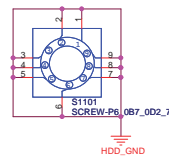
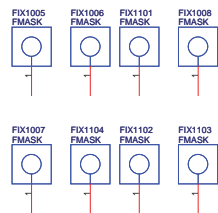
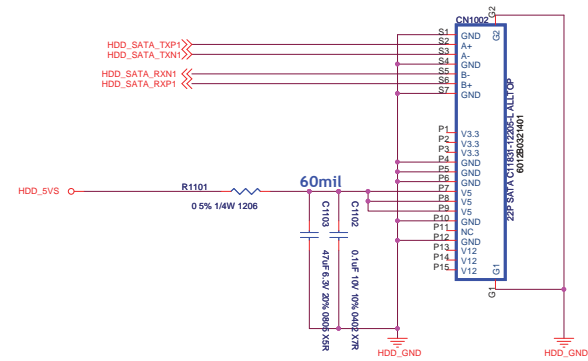
Page 47:
SW Gfx: Stuff
UMA: OPEN

INVENTEC				
TITLE BAP41/BAP51 (Montevina SFF) VGA Power				
SIZE Custom	CODE A02	DOC NUMBER D-CS-1310A2292001-ALG	REV A02	
CHANGE by Shan-Chin Chang		DATE Thursday, July 02, 2009	SHEET 47 of 49	

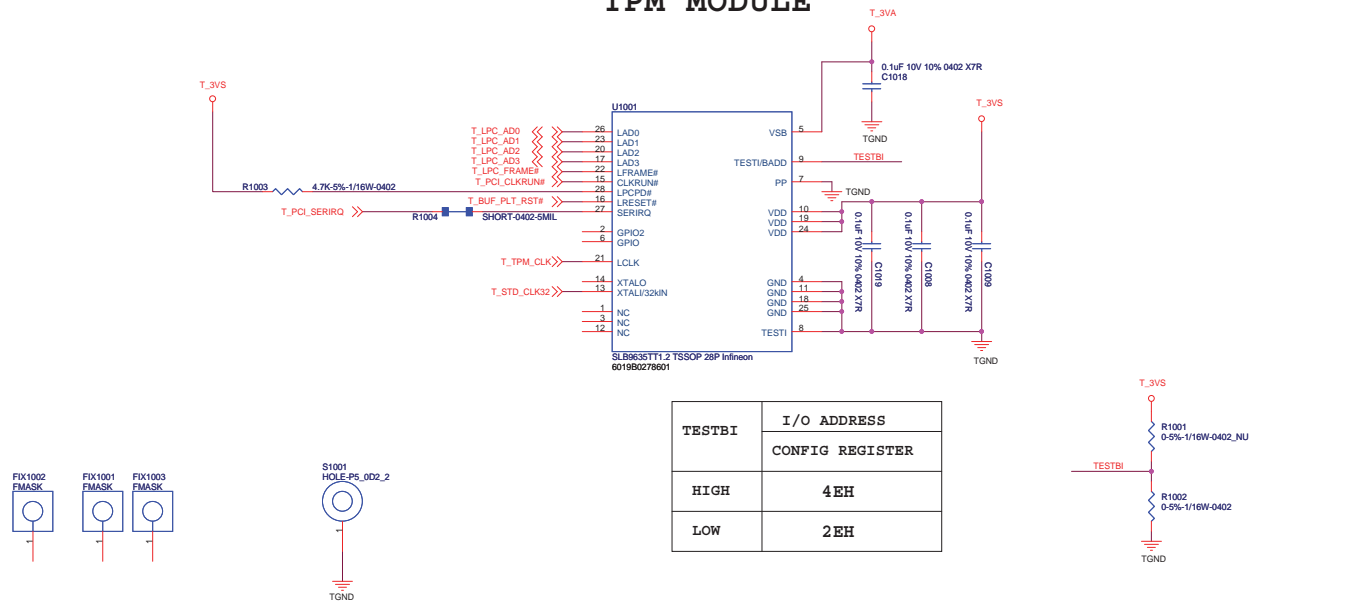
HDD Board CN TO MB



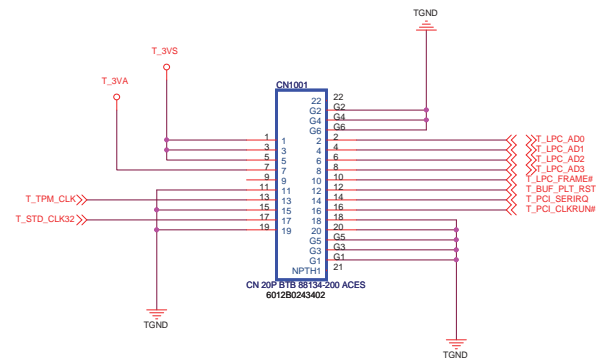
HDD I/F



TPM MODULE



TO MINI-CARD/B



INVENTEC

TITLE
BAP41/BAP51 (Montevina SFF)
TPM Board

SIZE CODE DOC NUMBER REV
Custom A02 D-CS-1310A2292001-ALG A02
SHEET 49 of 49